Remarks/Arguments:

The present invention relates to a digital signal receiver which includes a signal generator and a base-band transform circuit. Specifically, a frequency divider divides a reference signal and a frequency multiplier multiples the output of the divider. The output of the frequency multiplier is a product of the output signal of the divider and a magnitude of the frequency multiplier.

On page 2, the Official Action rejects claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Hayashi et al. (U.S. Patent No. 6,075,829).

Applicants claim 1 is different than Hayashi, because Applicant recites a **frequency multiplier** whereas Hayashi teaches a **heterodyning multiplier**. A frequency multiplier is functionally different than a heterodyning multiplier. Specifically, a frequency multiplier produces a sinusoid with a frequency that is a **product**. In contrast, a heterodyning multiplier produces two sinusoids with frequencies that are the **sum and difference**.

Hayashi teaches a digital broadcast receiver. Specifically, Hayashi teaches a reference signal that is divided in frequency and then outputted to a heterodyning multiplier.

Applicants' invention as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> **... a frequency multiplier wherein an output frequency of the frequency multiplier is a product of the divided first reference signal produced by the frequency divider and a magnitude of the frequency multiplier ...**

Claim 1 relates to a frequency multiplier which produces a frequency which is the product between an output frequency of a frequency divider and a magnitude of the frequency multiplier. This feature is found in the originally filed application on page 3, and furthermore in Fig. 1. No new matter has been added.

Fig. 1 of Hayashi shows frequency divider 35 and multiplier 11. Hayashi's multiplier 11, however, is a heterodyning multiplier (not a frequency multiplier). For example, heterodyning multiplier 11 (as taught by Hayashi) multiples a sinusoid output from oscillator 31 (for example **cos(F1)**) with another sinusoid from port 10 (for example **cos(F2)**). These two sinusoids are multiplied together in a heterodyning procedure wherein the output of the multiplier produces two new sinusoids with different frequencies. One of the new sinusoid frequencies produced by heterodyning multiplier 11 is at the sum of the two input frequencies (**F1 + F2**) and the other is at the difference of the two input frequencies (**F1 - F2**) (not the product of the two frequencies F1 * F2):

*cos (**F1**) * cos (**F2**) = .5 * ((cos (**F1 + F2**) +cos (**F1 - F2**))*

Applicants' claim 1 is different then Hayashi because the addition of a **frequency multiplier** which produces a frequency which is the **product** of the frequency divider output and a magnitude of the frequency multiplier. For example, in Applicants' Fig. 1, frequency multiplier 5 multiples the frequency of the sinusoid output of frequency divider 4. If the sinusoid output of frequency divider 4 has a frequency ***cos(Fin)***, and frequency multiplier 5 has a magnitude ***N***, then the frequency of the output sinusoid ***cos(Fout)*** of the frequency multiplier 5 would be the product of the two:

Frequency of divider output *cos(**Fin**)*

Magnitude of frequency multiplier ***N***

Product of frequency multiplier cos(***Fout***) = *cos(**Fin * N**)*

Thus, Hayashi's multiplier is a heterodyning multiplier which produces sinusoids with frequencies at the sum ***cos (F1 + F2)*** and difference ***cos (F1 - F2)*** of the input frequencies, whereas Applicants' frequency multiplier produces a sinusoid with a frequency that is the product between the input sinusoid frequency and the multiplier magnitude ***cos(Fin * N)***. Therefore, combining Hayashi and AAPA would not teach the features of Applicants' claim 1 (Hayashi's multiplier is not a frequency multiplier).

It is because Applicants include the feature of "*a frequency multiplier wherein an output frequency of the frequency multiplier is a product of the divided first reference signal produced by the frequency divider and a magnitude of the frequency multiplier*," that the following advantages are achieved. An advantage is to reduce the frequency of the signal that is input to the frequency multiplier, thus, reducing the buffer current that is needed. Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 2-10 include all of the features of claim 1 from which they depend. Thus, claims 2-10 are also patentable over the art of record for the reasons set forth above.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

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